WHAT IS CLAIMED IS:

Sub B1

[c1] 1. An apparatus comprising:

a tapped delay circuit including a plurality of tapped delay cells, said tapped delay circuit receiving a first pulse signal as input;

a plurality of sampling modules, each sampling module receiving a second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, and each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells;

and an encoder for generating an output value based on a number of sampling modules that lock into said second pulse signal.

[c2] 2. The apparatus of claim 1, wherein said output value represents the process, voltage, and temperature (PVT) conditions of a microchip.

[c3] 3. The apparatus of claim 1, further comprising:

an input for a clock signal;

a counter for counting the cycles of said clock signal;

wherein said encoder generates said output value during predefined intervals defined by said clock signal.

[c4] 4. The apparatus of claim 1, further comprising:

a variation circuit for receiving said generated output value generated and comparing said generated output value to a previously stored maximum output value and a previously stored minimum output value,

wherein if said generated output value is less than said previously stored minimum output value, said generated output value is stored as said minimum output value, and

wherein if said generated output value is greater than said maximum output value, said generated output value is stored as said maximum output value.

[c5] 5. The apparatus of claim 4, wherein said minimum output value and said maximum output value stored in said variation circuit represents a range of process, voltage, and temperature (PVT) conditions for a microchip.

[c6] 6. The apparatus of claim 1, wherein said plurality of tapped delay cells includes at least one DELC1V15 delay component.

[c7] 7. The apparatus of claim 1, further comprising:

a plurality of synchronizing elements for synchronizing the output signals from said plurality of sampling modules according to a clock signal,

wherein the outputs of said plurality of synchronizing elements are input to said encoder.

[c8] 8. A variable delay circuit comprising:

a variable delay component for delaying an input signal, said variable delay component having a delay time that is controlled according to a control signal;

a delay compensation circuit for measuring the process, voltage, and temperature (PVT) conditions of a microchip and outputting a value representative of said measured PVT conditions,

wherein said output value representative of said measured PVT conditions is used to generate said control signal for said variable delay component.

[c9] 9. The variable delay circuit of claim 8, wherein said variable delay component is a tapped delay circuit, which includes

a plurality of tapped delay cells connected in series;

and a multiplexor for selecting and outputting a tapped signal from one of said plurality of tapped delay cells based on said control signal.

[c10] 10. The variable delay circuit of claim 9, wherein said plurality of tapped delay cells includes at least one DELC1V15 delay component.

[c11] 11. The variable delay circuit of claim 8, wherein said delay compensation circuit includes

a tapped delay circuit including a plurality of tapped delay cells, said tapped delay circuit receiving a first pulse signal as input;

a plurality of sampling modules, each sampling module receiving a second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, and

each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells;

and an encoder for outputting said value representative of PVT conditions based on a number of sampling modules that lock into said second pulse signal.

[c12] 12. The variable delay circuit of claim 11, wherein said delay compensation circuit further includes

an input for a clock signal;

a counter for counting the cycles of said clock signal;

wherein said encoder generates said output value during predefined intervals defined by said clock signal.